REMARKS/ARGUMENTS

Favorable reconsideration of this application as currently amended and in view of the following discussion is respectfully requested.

Claims 1-4 are pending in the present application. Claims 1-3 are amended by the present amendment.

In the Advisory Action of January 20, 2006, the rejections of the Office Action of September 16, 2005, were maintained. In the Office Action of September 16, 2005, Claims 1-3 were rejected under 35 U.S.C. § 102(b) as anticipated by Shokouhi et al. (U.S. Patent No. 6,249,458, herein "Shokouhi"), and Claim 4 was rejected under 35 U.S.C. § 102(b) as anticipated by Javanifard et al. (U.S. Patent No. 5,455,794, herein "Javanifard").

Regarding the rejection of Claims 1-3 under 35 U.S.C. § 102(b) as anticipated by Shokouhi, independent Claim 1 has been amended to recite a plurality of disconnecting devices, each being individually connected to a disconnection control circuit such that the plurality of disconnecting devices are independently controlled by the disconnection control circuit. In addition, Claims 2 and 3 have been amended to be consistent with amended Claim 1. The claim amendments find support in Figure 3 and in the specification at page 11, lines 3-15. No new matter has been added.

Briefly recapitulating, amended Claim 1 is directed to a semiconductor memory that has a plurality of word lines, a plurality of bit lines, a plurality of memory cells, a Y decoder, and a plurality of disconnecting devices. Each memory cell is connected to one word line of the plurality of word lines and one bit line of the plurality of bit lines. The Y decoder drives the plurality of bit lines. The plurality of disconnecting devices are provided such that each disconnecting device is between at least one corresponding bit line of the plurality of bit lines and the Y decoder. Each disconnecting device is individually connected to a disconnection

control circuit such that the plurality of disconnecting devices are individually controlled by the disconnection control circuit.

In a non-limiting example, Figure 3 shows the semiconductor memory having the plurality of word lines 5 to 8, the plurality of bit lines 3 and 4, the plurality of memory cells 9 to 16, the Y decoder 1, the plurality of disconnecting devices 17 and 18, and the disconnection control circuit 20.

Turning to the applied art, Shokouhi shows in Figure 3 a memory device having a decoder 850 connected through disconnecting switches 840 to a plurality of bit lines BL0 to BLX. However, Shokouhi fails to teach or suggest that the disconnecting devices 840 are independently controlled by a disconnection control circuit. Figure 3 of Shokouhi suggests that the disconnecting switches 840 are connected to a single line CNTRL to be commonly controlled by a control circuit and are not individually controlled as required by amended Claim 1.

In addition, the Office Action of September 16, 2005, asserts in the paragraph bridging pages 2 and 3 that the disconnecting devices 840 of Shokouhi "operate in a manner similar to switches 830." However, the switches 830 shown in Figure 3 of Shokouhi are commonly controlled through a single line BLL by a switch BLL SWITCH 440, and are not individually connected to the control circuit 440 to be independently controlled as required by amended Claim 1.

Further, Shokouhi shows in Figure 8 a plurality of switches 813 being controlled by the single switch BLL SWITCH 440 through only a single line BLL. Thus, the switches 813 also cannot be independently controlled as requested in amended Claim 1.

Accordingly, it is respectfully submitted that amended Claim 1 and each of the claims depending therefrom patentably distinguish over Shokouhi.

Regarding the rejection of Claim 4 under 35 U.S.C. § 102(b) as anticipated by Javanifard, that rejection is respectfully traversed for the following reasons.

The Office Action of September 16, 2005, relies on Figures 2 and 3 of Javanifard for showing various claimed elements and combines the teachings of Figures 2 and 3 as described in the first full paragraph on page 5 of the Office Action of September 16, 2005. As noted in the previously filed amendment, a rejection under 35 U.S.C. § 102 is improper when distinct embodiments of a same reference are combined.

However, assuming that the combination of the two different embodiments shown respectively in Figures 2 and 3 of Javanifard is proper, Applicant respectfully submits that the combination of Figure 2 and 3 of Javanifard discloses a terminal 31 connected through a first switch 35, a voltage pump 32, and a second switch 36 to a memory EEPROM. However, Claim 4 recites that a charge pump is connected to a Y decoder through a first switching circuit and a port circuit is connected to the Y decoder through a second switching circuit. Figure 5 shows the port circuit 101 not connected through the pump 100 and the first switching circuit 103 as is the case in Javanifard.

In other words, Javanifard connects the terminal 31 and the pump 32 in series to the decoder while the memory of Claim 4 has the port circuit and the charge pump connected in parallel to the Y decoder.

For the above noted reasons, Applicant respectfully submits that Claim 4 patentably distinguishes over Javanifard.

Consequently, in light of the above discussion and in view of the present amendment, the present application is believed to be in condition for allowance and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

Eckhard H. Kuesters
Attorney of Record
Registration No. 28,870
Remus F. Fetea, Ph.D.
Limited Recognition No. L0037

Customer Number
22850

Tel: (703) 413-3000
Fax: (703) 413 -2220
(OSMMN 06/04)

EHK/RFF/ys
I:\ATTY\RFF\24S\244299\244299-AME-JAN25.DOC